What is Claimed is:

1. A field effect transistor comprising:

a fin extending from a substrate, the fin including an upper portion remote from the substrate and sidewalls that extend between the upper portion and the substrate;

a channel region in the fin;

a gate electrode adjacent the channel region and crossing over the fin;

a gate insulation layer interposed between the gate electrode and the fin; and

source/drain regions formed at both sides of the gate electrode, wherein the channel region at the upper portion of the fin is doped higher than sidewalls of the fin.

2. The transistor of Claim 1, wherein the channel region comprises:

a first layer in the upper portion of the fin; and

a second layer beneath the first layer, wherein the second layer is lightly doped relative to the first layer.

3. The transistor of Claim 1:

wherein the substrate includes a semiconductor layer and an insulation layer on the semiconductor layer; and

wherein the fin is on the insulation layer.

4. The transistor of Claim 1:

wherein the substrate is a bulk semiconductor layer; and

wherein the semiconductor layer extends vertically to form the fin.

5. The transistor of Claim 4, further comprising an insulation layer disposed between the gate electrode and the semiconductor layer at a periphery of the fin.

6. The transistor of Claim 4, further comprising a punch-through stop layer beneath the channel region having a higher doping concentration than the second layer.

7. The transistor of Claim 2, wherein the second layer has uniform concentration in the channel region.

8. A method of fabricating an integrated circuit transistor comprising:

forming a fin extending vertically from a substrate;

implanting a first impurity in an upper portion of the fin;

implanting a second impurity in an entire exposed surface of the fin;

forming a gate insulation layer on the fin;

forming a gate electrode crossing over the fin on the gate insulation layer;

wherein a first layer comprised of the first and second impurities is formed in the upper portion of the fin;

wherein a second layer comprising the second impurity is formed in the fin under the first layer; and

wherein the second layer is lightly doped relative to the first layer.

9. The method of Claim 8, further comprising implanting a third impurity in the fin beneath the gate electrode.

10. The method of Claim 8, wherein the second impurity is implanted using an oblique ion implantation.

11. The method of Claim 8, wherein the fin is formed by patterning a semiconductor layer of the substrate comprised of a stacked structure of an insulation layer and the semiconductor layer on a support substrate.

12. The method of Claim 8, wherein forming the fin comprises:

patterning a bulk substrate comprised of the semiconductor layer to form a portion extending vertically;

forming an insulation layer on the substrate; and

recessing the insulation layer to form the fin projecting from the insulation layer.

13. An integrated circuit field effect transistor comprising:

an integrated circuit substrate;

a fin that projects away from the integrated circuit substrate, extends along the integrated circuit substrate and includes a top that is remote from the integrated circuit substrate;

a channel region in the fin that is doped a predetermined conductivity type and having a higher doping concentration of the predetermined conductivity type adjacent the top than remote from the top;

a source region and a drain region in the fin on respective opposite sides of the channel region; and

an insulated gate electrode that extends across the fin, adjacent the channel region.

14. The integrated circuit field effect transistor according to Claim 13 wherein the channel region is uniformly doped the predetermined conductivity type at a first doping concentration except for being doped the predetermined conductivity type at a second doping concentration that is higher than the first doping concentration adjacent the top.

15. The integrated circuit field effect transistor according to Claim 13 wherein the channel region comprises a first region of the predetermined conductivity type adjacent the top and a second region of the predetermined conductivity type remote from the top, wherein the first region is more heavily doped than the second region.

16. The integrated circuit field effect transistor according to Claim 13 wherein the fin also includes first and second sidewalls that extend between the top and the substrate and wherein the channel region has the higher doping concentration of the predetermined conductivity type directly beneath the top, from the first sidewall to the second sidewall.

17. The integrated circuit field effect transistor according to Claim 13:

wherein the integrated circuit substrate is a bulk semiconductor substrate such that the bulk semiconductor substrate includes a projection that defines the fin;

the integrated circuit field effect transistor further comprising a region of the predetermined conductivity type in the bulk semiconductor substrate beneath the fin.

18. The integrated circuit field effect transistor according to Claim 13 wherein the integrated circuit substrate comprises an insulating layer on a substrate and wherein the fin is on the insulating layer, opposite the substrate.

19. The integrated circuit field effect transistor according to Claim 13 further comprising:

a capacitor connected to the source region.

20. The integrated circuit field effect transistor according to Claim 13 further comprising:

a bit line connected to the drain region.

21. A method of fabricating an integrated circuit field effect transistor comprising:

forming a fin that projects away from an integrated circuit substrate, extends along the integrated circuit substrate and includes a top that is remote from the integrated circuit substrate;

implanting ions of a predetermined conductivity type into the fin orthogonal to the substrate;

implanting ions of the predetermined conductivity type into the fin oblique to the substrate; and

forming spaced apart source and drain regions in the fin and an insulated gate on the fin.

22. A method according to Claim 21 further comprising:

again implanting ions of the predetermined conductivity type into the fin orthogonal to the substrate.